TAA2008

STEREO 9W (8Ω) CLASS-T™ DIGITAL AUDIO AMPLIFIER USING DIGITAL POWER PROCESSING™ TECHNOLOGY

TECHNICAL INFORMATION **Revision 1.0 – May 2006**

GENERAL DESCRIPTION

The TAA2008 is a 9W/ch continuous average two-channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. The TAA2008, in a QFN package, along with extremely high efficiency, allows for a very compact amplifier design. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

APPLICATIONS

- LCD TV's
- LCD Monitors
- Plasma TV's
- Computer/PC Multimedia
- Battery Powered Systems

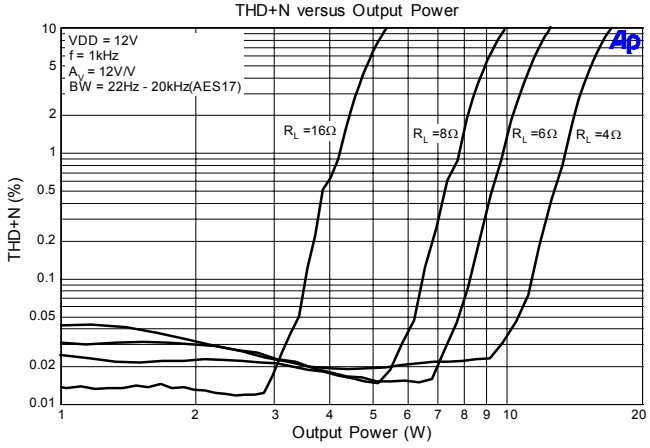
BENEFITS

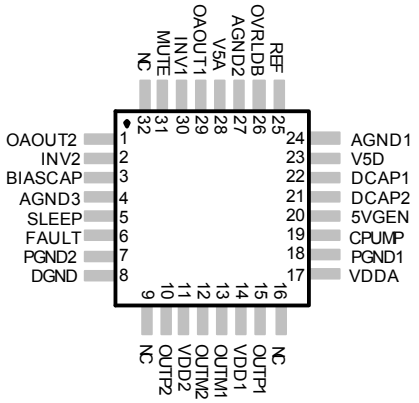
- Fully integrated solution with FETs
- Compact packaging and board design
- Reduced system cost with no heat sink
- Dramatically improves efficiency versus Class-AB
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD, DVD, and Internet audio
- Capable of driving a wide range of load impedances

FEATURES

- Class-T architecture
- Single Supply Operation
- "Audiophile" Quality Sound
- 0.025% THD+N @ 5W, 8Ω
- 0.1% IHF-IM @ 1W, 8Ω
- 6.3W @ 8Ω, 0.1% THD+N
- 3.5W @ 16Ω, 0.1% THD+N
- High Power
- 14.25W @ 6Ω, 10% THD+N
- 9W @ 8Ω, 10% THD+N
- 5W @ 16Ω, 10% THD+N
- Extremely High Efficiency
- 89% @ 5W, 16Ω
- 86% @ 9W, 8Ω
- Dynamic Range = 98.5 dB
- Mute and Sleep modes
- Improved turn-on & turn-off pop suppression
- Over-current protection with automatic restart circuit
- Over-temperature protection
- Space saving 32-pin 8mm x 8mm x 1mm QFN package with exposed pad

TYPICAL PERFORMANCE





ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	PARAMETER	Value	UNITS
V_{DD}	Supply Voltage	16	V
V5	Input Section Supply Voltage	6.0	V
SLEEP	SLEEP Input Voltage	-0.3 to 6.0	V
MUTE	MUTE Input Voltage	-0.3 to V5+0.3	V
T_{STORE}	Storage Temperature Range	-40 to 150	°C
T_A	Operating Free-air Temperature Range	0 to 70	°C
T_J	Junction Temperature	150	°C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 2)	2000	V
ESD_{MM}	ESD Susceptibility – Machine Model (Note 3)	200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 3: Machine model, 220pF – 240pF discharged through all pins.

OPERATING CONDITIONS (Note 4)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD}	Supply Voltage (Note 5)	8.5	12	14.0	V
V_{IH}	High-level Input Voltage (MUTE, SLEEP)	3.5			V
V_{IL}	Low-level Input Voltage (MUTE, SLEEP)			1	V

Note 4: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.
Note 5: Operation above 13.2V requires the use of low and high side schottky diodes as well as 220uF for C_{SW}. See the Application Section for additional information

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNITS
θ_{JA}	Junction-to-ambient Thermal Resistance (note 6)	22	°C/W

Note 6: The θ_{JA} value is based on the exposed pad being soldered down to the printed circuit board. The exposed pad must be soldered to an exposed copper area on the printed circuit board for proper thermal and electrical performance.

ELECTRICAL CHARACTERISTICS (Note 7)

See Test/Application Circuit. Unless otherwise specified, V_{DD} = 12V, f = 1kHz, Measurement Bandwidth = 20kHz, R_L = 8Ω, T_A = 25 °C, package exposed pad soldered to the printed circuit board.

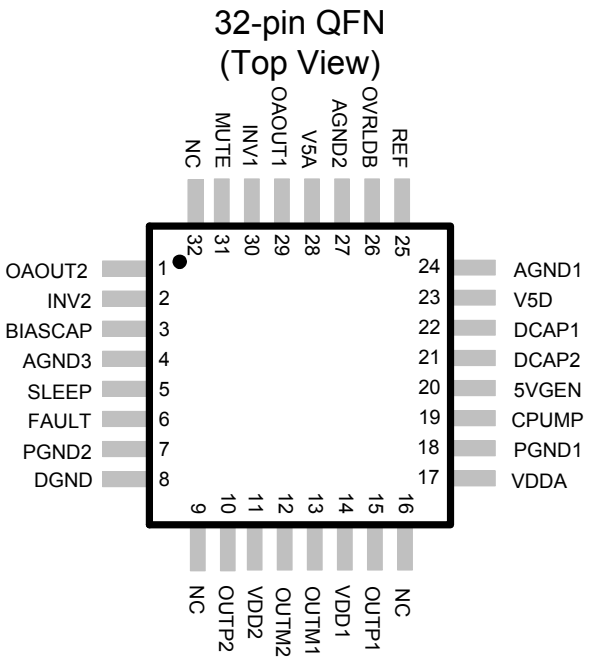
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_O	Output Power (Continuous Average/Channel)	THD+N = 0.1% R_L = 6Ω		8		W
		R_L = 8Ω		6.3		W
		R_L = 16Ω		3.5		W
		THD+N = 10% R_L = 6Ω		12		W
		R_L = 8Ω	TBD	9		W
		R_L = 16Ω		5		W
		VDD = 13.2V, THD+N=10%				
		R_L = 6Ω		14.25		W
		R_L = 8Ω		12		W
		R_L = 16Ω		6.3		W
$I_{DD,MUTE}$	Mute Supply Current	MUTE = V_{IH}		31	36	mA
$I_{DD, SLEEP}$	Sleep Supply Current	SLEEP = V_{IH}		0.25	2	mA
I_q	Quiescent Current	V_{IN} = 0 V		61	75	mA
THD + N	Total Harmonic Distortion Plus Noise	P_O = 5W/Channel		0.022		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF)		0.1	0.5	%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 9W, R_L = 8Ω		98.5		dB
CS	Channel Separation	f = 1 kHz		85		dB
		20 Hz ≤ f ≤ 20 kHz	50	60		dB
PSRR	Power Supply Rejection Ratio	VDD = 9V to 13.2V	65	75		dB
		Vripple = 100mVrms, f=1kHz		65		dB
η	Power Efficiency	P_{OUT} = 5W/Channel, R_L = 16Ω		89		%
V_{OFFSET}	Output Offset Voltage	No Load, MUTE = Logic Low		50	150	mV
V_{OH}	High-level output voltage (FAULT & OVERLOAD)		3.5			V
V_{OL}	Low-level output voltage (FAULT & OVERLOAD)				1	V
e_{OUT}	Output Noise Voltage	A-Weighted, input AC grounded		100	150	μV

Note 7: Minimum and maximum limits are guaranteed but may not be 100% tested.

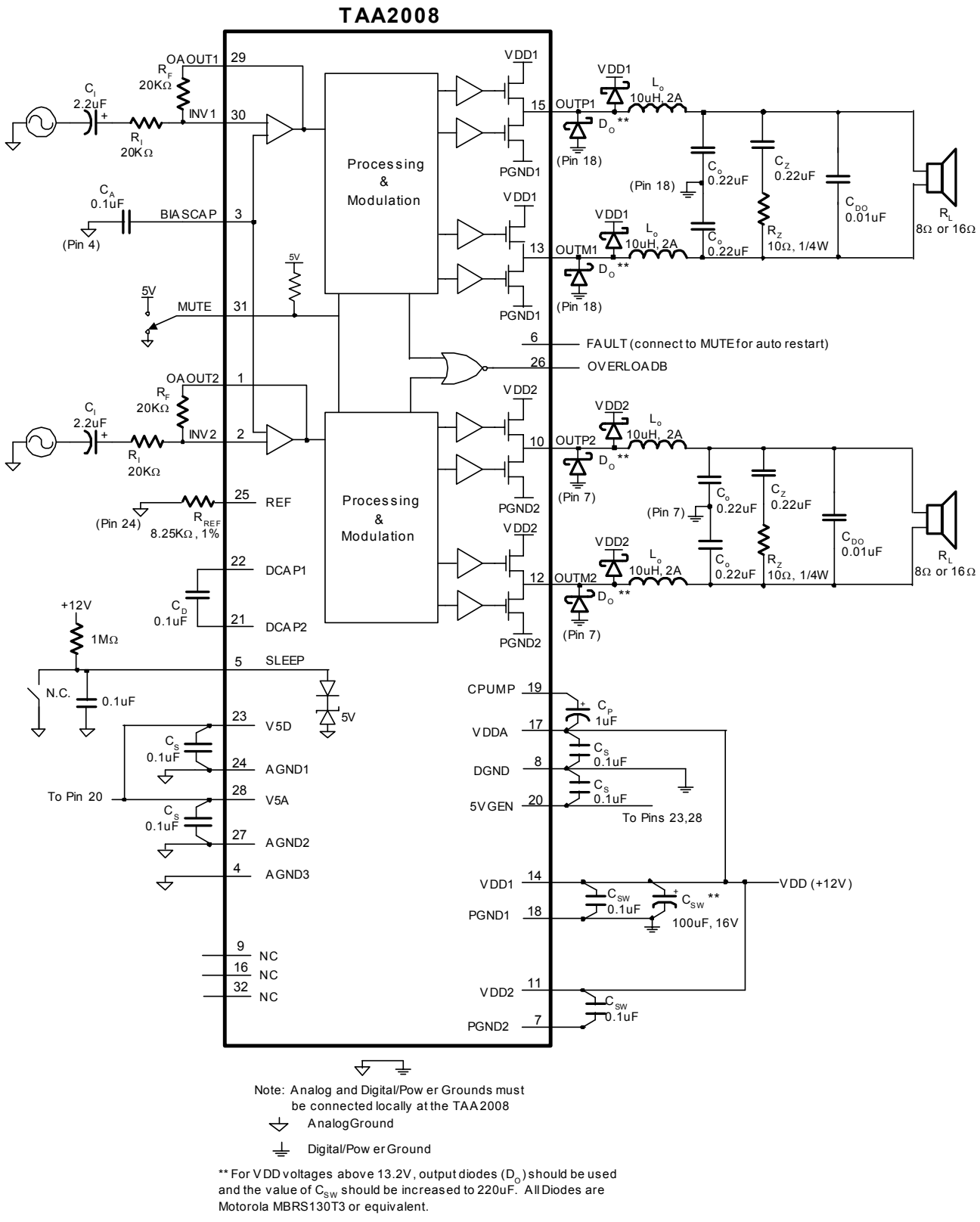
PIN DESCRIPTION

Pin	Function	Description
1, 29	OAOUT2, OAOUT1	Input stage output pins.
2, 30	INV2, INV1	Single-ended inputs. Inputs are a “virtual” ground of an inverting opamp with approximately 2.4VDC bias.
3	BIASCAP	Input stage bias voltage (approximately 2.4VDC).
4, 24, 27	AGND3, AGND1, AGND2	Analog Ground
5	SLEEP	When set to logic high, device goes into low power mode. If not used, this pin should be grounded
6	FAULT	A logic high output indicates thermal overload, or an output is shorted to ground, or another output.
7, 18	PGND2, PGND1	Power Grounds (high current)
8	DGND	Digital Ground. Connect to AGND locally (near the TAA2008).
10, 12; 15, 13	OUTP2 & OUTM2; OUTP1 & OUTM1	Bridged output pairs
11, 14	VDD2, VDD1	Supply pins for high current H-bridges, nominally 12VDC.
17	VDDA	Analog 12VDC. Connect to same supply as VDD1 and VDD2.
19	CPUMP	Charge pump output (nominally 10V above VDDA)
20	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 23 and 28).
21,22	DCAP2, DCAP1	Charge pump switching pins. DCAP1 (pin 22) is a free running 300kHz square wave between VDDA and DGND (12Vpp nominal). DCAP2 (pin 21) is level shifted 10 volts above DCAP1 (pin 22) with the same amplitude (12Vpp nominal), frequency, and phase as DCAP1.
23, 28	V5D, V5A	Digital 5VDC, Analog 5VDC
25	REF	Internal reference voltage; approximately 1.0 VDC.
26	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier.
31	MUTE	When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. This pin should be tied to GND if not used.
9, 16, 32	NC	Not connected. Not bonded internally.

TAA2008 PINOUT



APPLICATION / TEST CIRCUIT



Note: Analog and Digital/Power Grounds must be connected locally at the TAA2008

Analog Ground

Digital/Power Ground

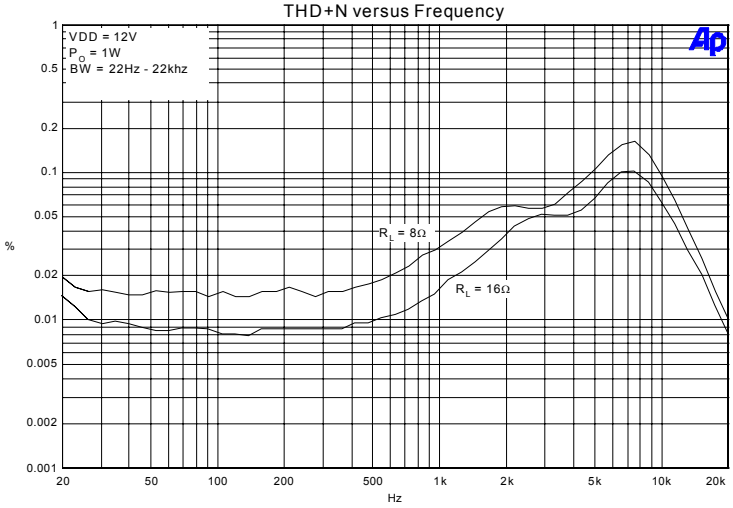
** For VDD voltages above 13.2V, output diodes (D_O) should be used and the value of C_{SW} should be increased to 220uF. All Diodes are Motorola MBRS130T3 or equivalent.

EXTERNAL COMPONENTS DESCRIPTION (Refer to the Application/Test Circuit)

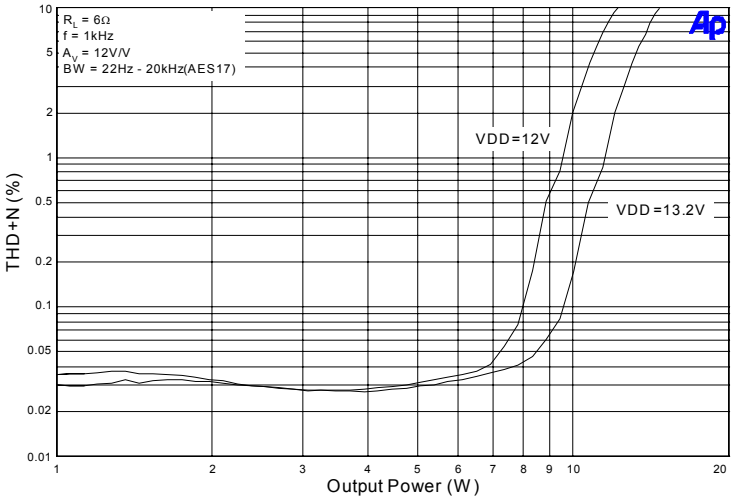
Components	Description
R_I	Inverting Input Resistance to provide AC gain in conjunction with R_F. This input is biased at the BIASCAP voltage (approximately 2.4VDC).
R_F	Feedback resistor to set AC gain in conjunction with R_I; $A_V = 12(R_F / R_I)$. Please refer to the Amplifier Gain paragraph in the Application Information section.
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a highpass filter at $f_C = 1/(2\pi R_I C_I)$
R_{REF}	Bias resistor. Locate close to pin 25 (REF) and ground at pin 24 (AGND1).
C_A	BIASCAP decoupling capacitor. Locate close to pin 3 (BASCAP) and ground at pin 4 (AGND3).
C_D	Charge pump input capacitor. This capacitor should be connected directly between pins 21 (DCAP2) and 22 (DCAP1) and located physically close to the TAA2008.
C_P	Charge pump output capacitor that enables efficient high side gate drive for the internal H-bridges. To maximize performance, this capacitor should be connected directly between pin 19 (CPUMP) and pin 17 (VDDA). Please observe the polarity shown in the Application/ Test Circuit.
C_S	Supply decoupling for the low current power supply pins. For optimum performance, these components should be located close to the pin and returned to their respective ground as shown in the Application/Test Circuit.
C_{SW}	Supply decoupling for the high current, high frequency H-Bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. Both the high frequency bypassing (0.1uF) and bulk capacitor (100uF/220uF) should have good high frequency performance including low ESR and low ESL. Recommended capacitor families include Nichicon HE series and Panasonic FM series for thru-hole types. Qualified SMT electrolytics include Nichicon UD series and Panasonic FK series.
C_Z	Zobel Capacitor.
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with frequency.
D_O	Schottky diodes that minimize undershoots and overshoots of the outputs with respect to power ground and VDD during switching transitions. These components are recommended for supply voltages above 13.2V. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective PGND. Please see Application/Test Circuit for ground return pin.
L_O	Output inductor, which in conjunction with C_O and C_{DO}, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_{TOT}})$ and a quality factor of $Q = R_L C_{TOT} / 2\sqrt{L_O C_{TOT}}$ where $C_{TOT} = C_O \parallel 2 * C_{DO}$.
C_O	Output capacitor.
C_{DO}	Differential Output Capacitor. Differential noise decoupling for reduction of conducted emissions. Must be located near chassis exit point for maximum effectiveness.

TYPICAL PERFORMANCE

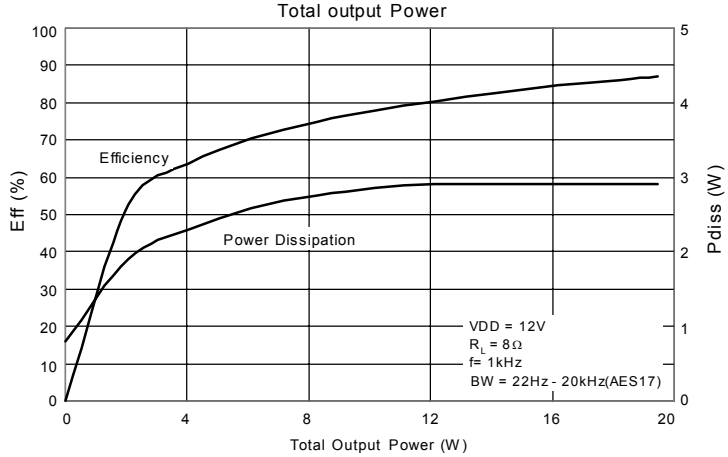
THD+N versus Frequency



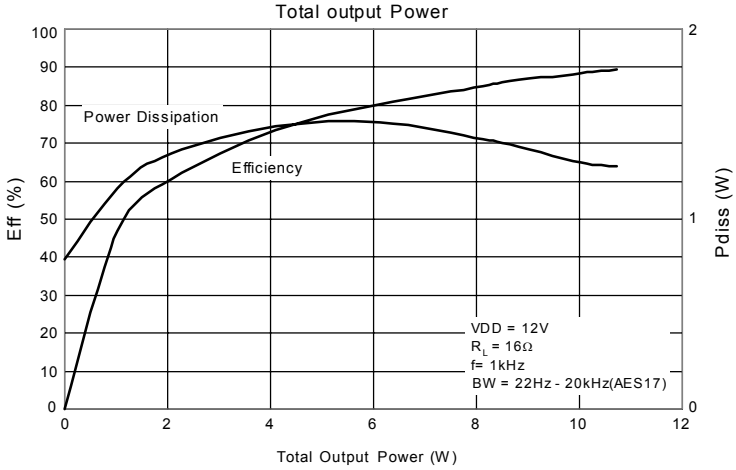
THD+N versus Output Power



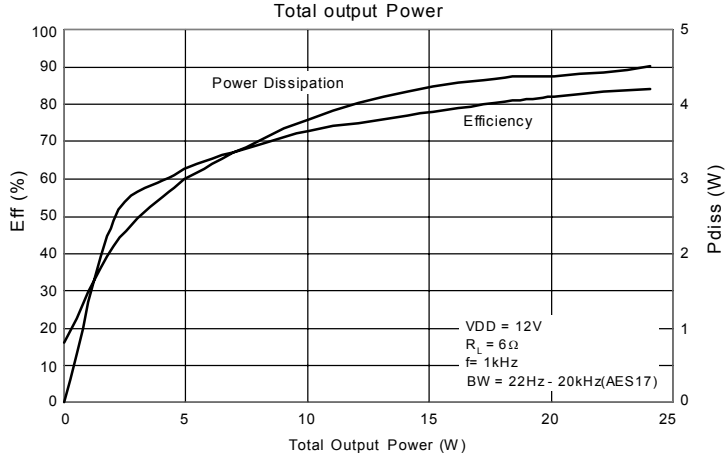
Efficiency and Power Dissipation versus Total output Power



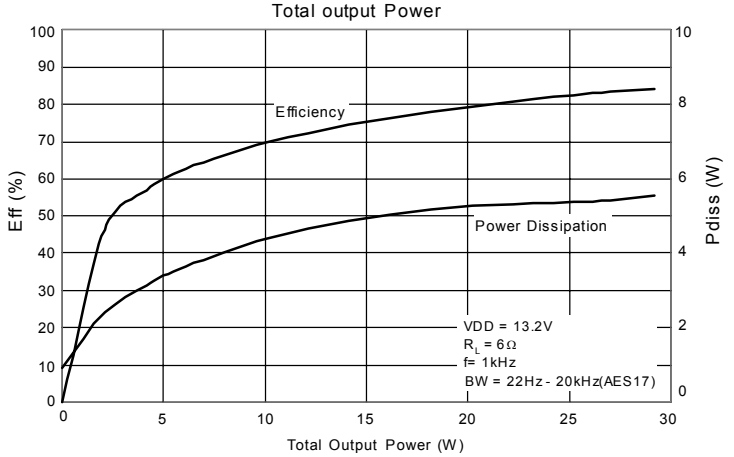
Efficiency and Power Dissipation versus Total output Power



Efficiency and Power Dissipation versus Total output Power

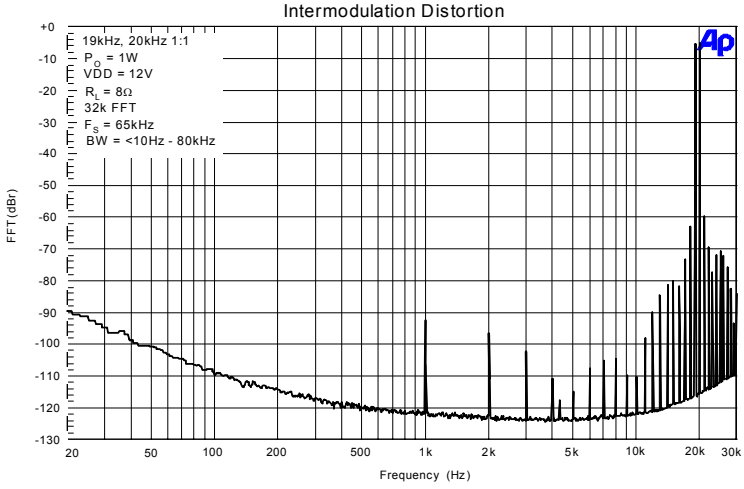


Efficiency and Power Dissipation versus Total output Power

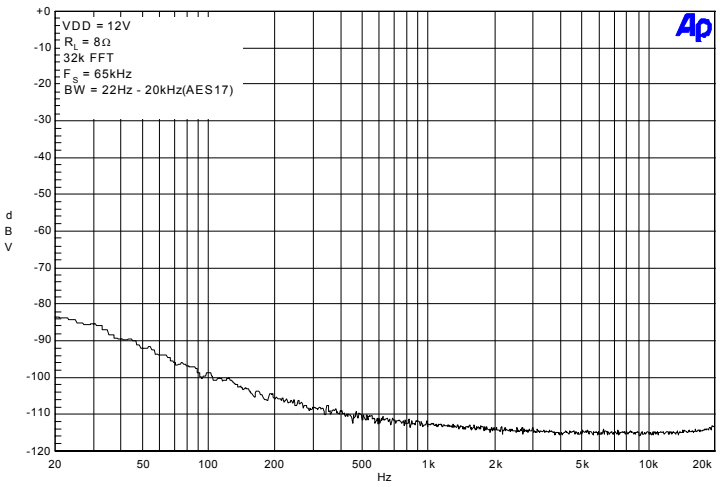


TYPICAL PERFORMANCE

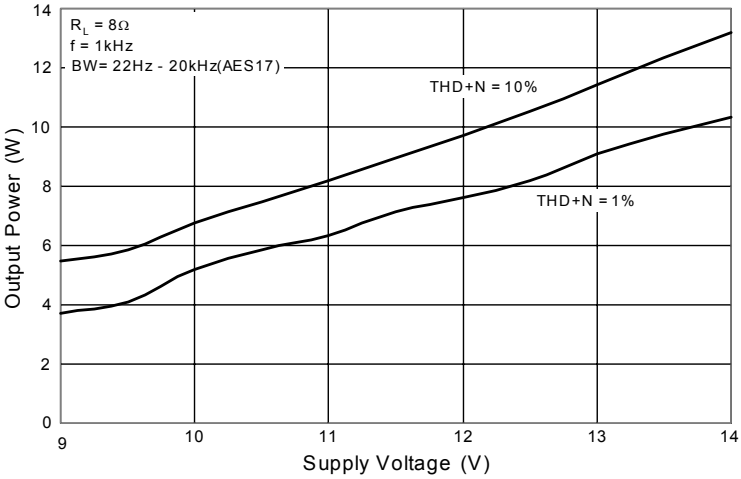
Intermodulation Distortion



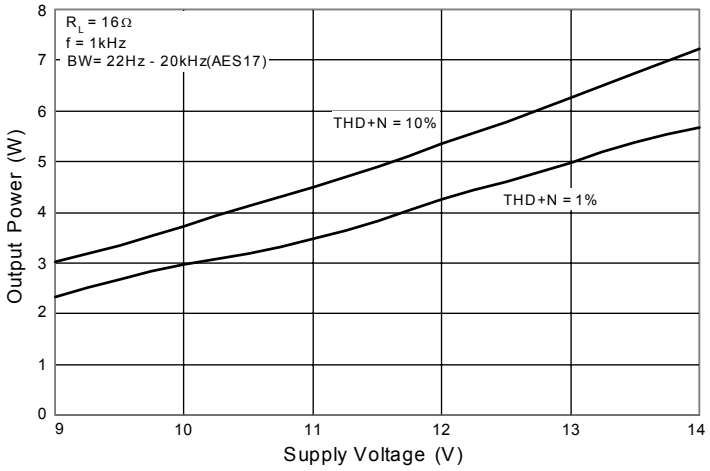
Noise Floor



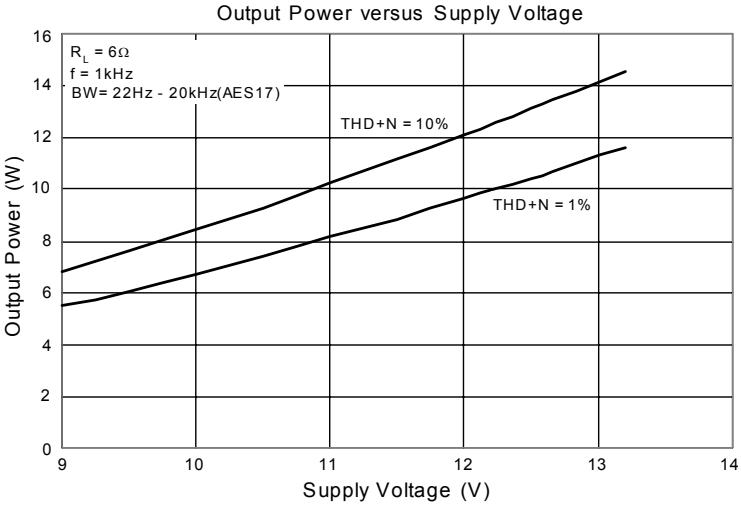
Output Power versus Supply Voltage



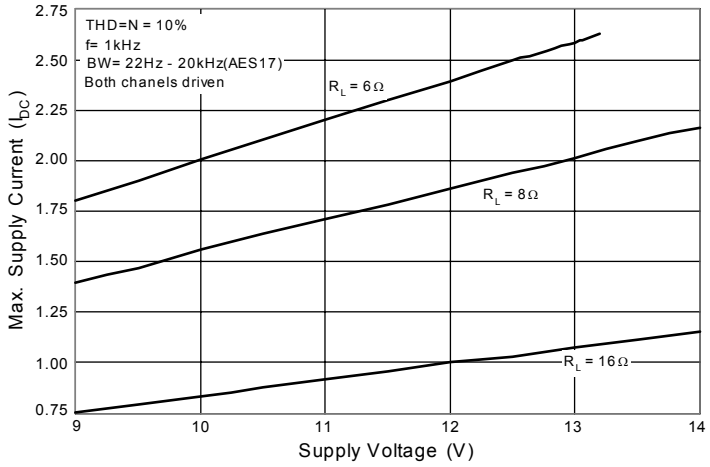
Output Power versus Supply Voltage



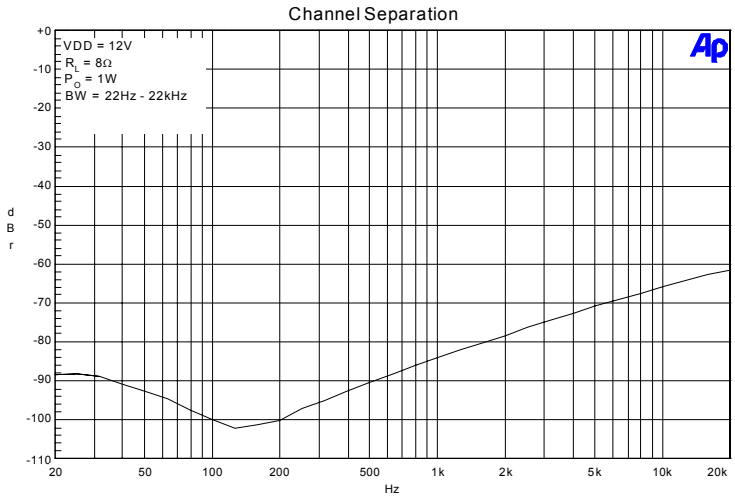
Output Power versus Supply Voltage

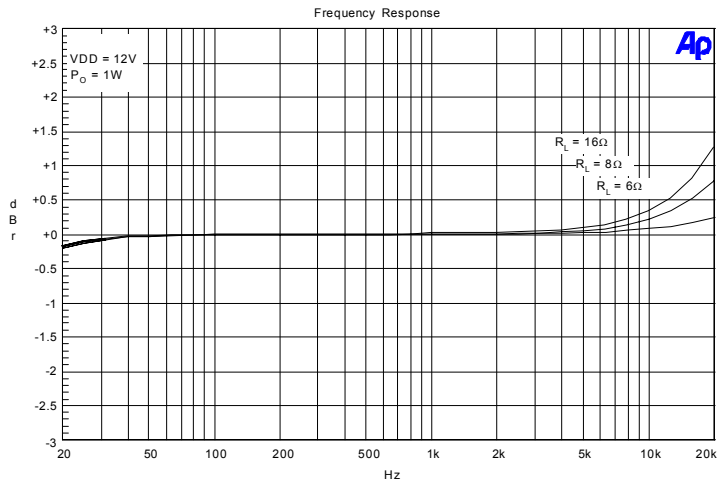


Maximum Supply Current versus Supply Voltage



TYPICAL PERFORMANCE





APPLICATION INFORMATION

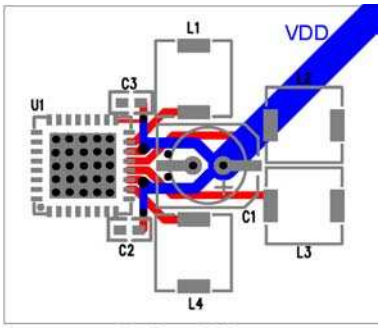
Layout Recommendations

The TAA2008 is a power (high current) amplifier that operates at relatively high switching frequencies. The outputs of the amplifier switch between the supply voltage and ground, at high speeds, while driving high currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TAA2008 to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes. Please contact Tripath Technology for further information regarding reference design material regarding the TAA2008.

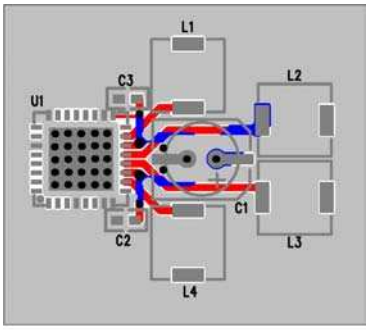
Output Stage layout Considerations and Component Selection Criteria

Proper PCB layout and component selection is a major step in designing a reliable TAA2008 power amplifier. The supply pins require proper decoupling with correctly chosen components to achieve optimal performance and reliability.

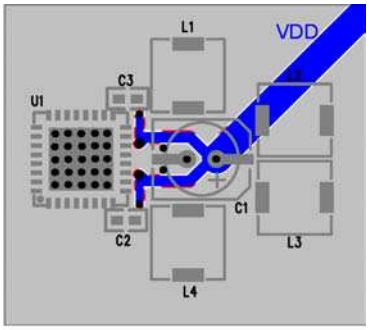
The output pins need proper protection to keep the outputs from going below ground and above VDD.



Top Trace RED
Bottom Trace BLUE
Via BLACK
All Components TOP



Top Trace RED
Bottom Trace BLUE
Top Copper GRAY
Via BLACK
All Components TOP



Top Trace RED
Bottom Trace BLUE
Bottom Copper GRAY
Via BLACK
All Components TOP

The above layout shows ideal component placement and routing for supply decoupling. C2 and C3 are .1uF surface mount capacitors placed directly across their respective VDD and PGND pins. C1 is a low ESR bulk capacitance electrolytic (at least 100uF). C1's VDD pin is routed to the TAA2008's VDD1 and VDD2 pins on the opposite side of the PCB as the TAA2008. Vias return the supply trace to the TAA2008 side of the PCB at the VDD1 and VDD2 pins. This arrangement allows C1's PGND pin to have a low impedance return path to PGND1 and PGND2 through the PCB's ground plane and allows the output traces (OUTM1, OUTP1, OUTM2, AND OUTP2) to be routed directly to the low pass filter. By having C1's supply pins directly across the TAA2008's VDD and PGND pins supply overshoots will be controlled and mean supply elevation will be reduced. Effectively decoupling VDD will shunt any power supply trace length inductance.

The construction of the bulk electrolytic is critical. This capacitor should be a low ESR, ripple rated SMT, or through-hole component. Water based through-hole electrolytic capacitors offer very cost competitive solutions with extremely low impedance (ESR). These include Nichicon HE series and Panasonic FM series. Qualified SMT electrolytics include Nichicon UD series and Panasonic FK series. Panasonic FC capacitors also work well but are likely more costly with no improvement in performance over the capacitor families mentioned above.

The output L1 – L4 should be placed close to the TAA2008 without compromising the locations of the closely placed supply decoupling capacitors. The purpose of placing the inductors close to the TAA2008 output pins in to reduce the trace length of the switching outputs. This will aid in reducing radiated emissions.

For VDD voltages above 13.2V, or on designs where a tight layout cannot be adhered to due to physical constraints, it is strongly recommended that the value of C_{SW} is increased to 220uF and that both low and high side schottky diodes are implemented. These changes will ensure that the output over shoots will not exceed the absolute maximum rating of 16V. The output diodes, D_O, should be located as close to the output pins as possible and returned to their respective PGND or VDD, as shown in the Application / Test Diagram.

Please see the External Component Description section on page 6 for more details on the above-mentioned components. The Application/ Test Circuit refers to both supply decoupling capacitors as C_{SW}, and the output diodes as D_O.

TAA2008 Amplifier Gain

The ideal gain of the TAA2008 is set by the ratio of two external resistors, R_I and R_F, and is given by the following formula:

$$\frac{V_O}{V_I} = -12\,\frac{R_F}{R_I}$$

where V_I is the input signal level and V_O is the differential output signal level across the speaker. Please note that V_O is 180° out of phase with V_I.

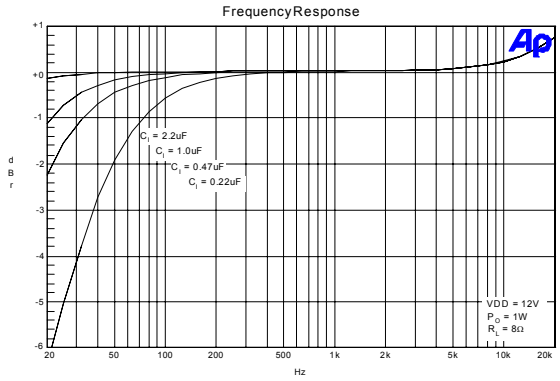
The ideal gain of the TAA2008 is 12V/V, whereas typical values are: A_V = 11.7V/V for 8Ω.

The low frequency roll-off characteristic is dictated by the choice of C_I and R_I.

The –3dB frequency is:

$$f_{-3dB} = \frac{1}{2\Pi C_I R_I}$$

The figure below shows the roll-off characteristic for different values of C_I, assuming an R_I value of 20kΩ. As can be seen, the larger the value of C_I, the lower the –3dB cutoff point. On the EB-TAA2008, a value of 2.2μF is used for C_I which creates a nearly flat response down to 20Hz. In many cases, a lower value of C_I can be used because the speakers used in LCD TV's or similar applications do not have the ability to reproduce low frequency signals.



Mute Pin

The mute pin must be driven to a logic low or logic high state for proper operation. To enable the amplifier, connect the mute pin to a logic low. To enable the mute function, connect the mute pin to a logic high signal. Please note that the mute pin is a 5V CMOS input pin and the mute signal should be de-bounced to eliminate a possibility of falsely muting.

When in mute, the internal processor bias voltages are still active in the TAA2008. This minimizes any turn on pop caused by charging the input coupling capacitor. It is recommended that the mute is held high during power up or power down to eliminate audible transients.

If turn-on and/or turn-off noise is still present with a TAA2008 amplifier, the cause may be other circuitry external to the TAA2008 such as an audio processor or preamp. Multiple audio processors used in LCD TV's create audible pops as their power supply collapses. If the TAA2008 is still active (mute pin is low), then these audible pops will be amplified and output to the speakers. To eliminate this problem, simply activate the mute before the power supply collapses. The delay going into mute is approximately 1us, as compared to several hundred milliseconds on the previous Tripath IC's such as TA2024B.

Sleep Pin

The SLEEP pin is a 5V logic input that when pulled high (>3.5V) puts the part into a low quiescent current mode. This pin is internally clamped by a zener diode to approximately 6V thus allowing the pin to be pulled up through a large valued resistor (1MΩ recommended) to V_{DD}. To disable SLEEP mode, the sleep pin should be grounded.

Protection Circuits

The TAA2008 is guarded against over-temperature and over-current conditions. When the device goes into an over-temperature or over-current state, the FAULT pin goes to a logic HIGH state indicating a fault condition. When this occurs, the amplifier is muted, all outputs are TRI-

STATED, and will float to 1/2 of V_{DD}. The FAULT pin can be connected directly to MUTE to automatically recover from an overcurrent condition.

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 155°C. The thermal hysteresis of the part is approximately 45°C, therefore the fault will automatically clear when the junction temperature drops below 110°C.

Over-current Protection

An over-current fault occurs if more than approximately 7 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground. An over-current fault sets an internal latch that can only be cleared if the MUTE pin is toggled or if the part is powered down. Alternately, if the MUTE pin is connected to the FAULT pin, the HIGH output of the FAULT pin will toggle the MUTE pin and automatically reset the fault condition.

Overload

The OVRLDB pin is a 5V logic output. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVRLDB signal can be used to control a distortion indicator light or LED through a simple buffer circuit, as the OVRLDB cannot drive an LED directly.

Fault Pin

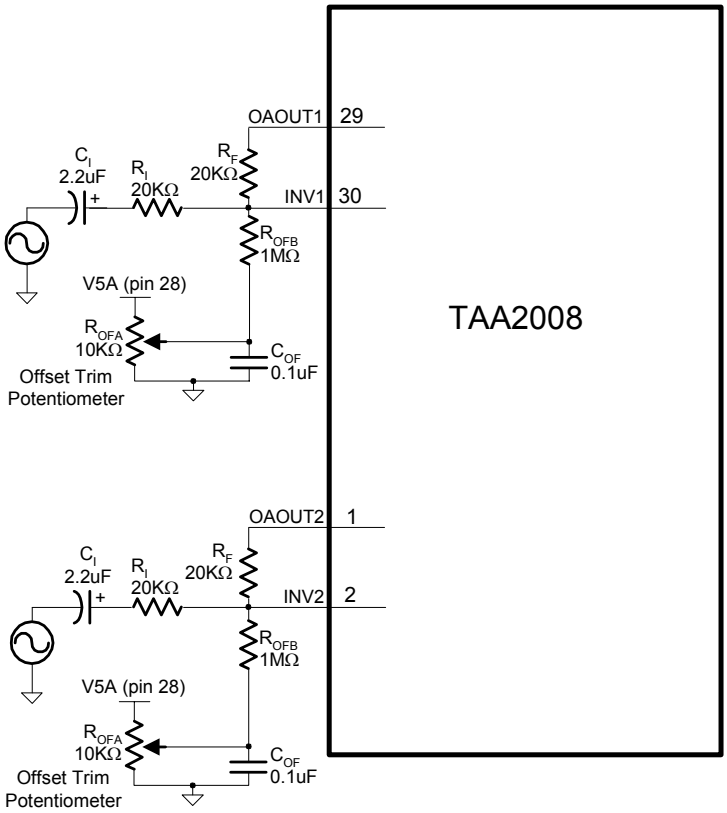
The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. All faults except overcurrent automatically reset upon removal of the condition. The FAULT output is capable of directly driving an LED through a series 2kΩ resistor. If the FAULT pin is connected directly to the MUTE input an automatic reset will occur in the event of an over-current condition.

Output Voltage Offset

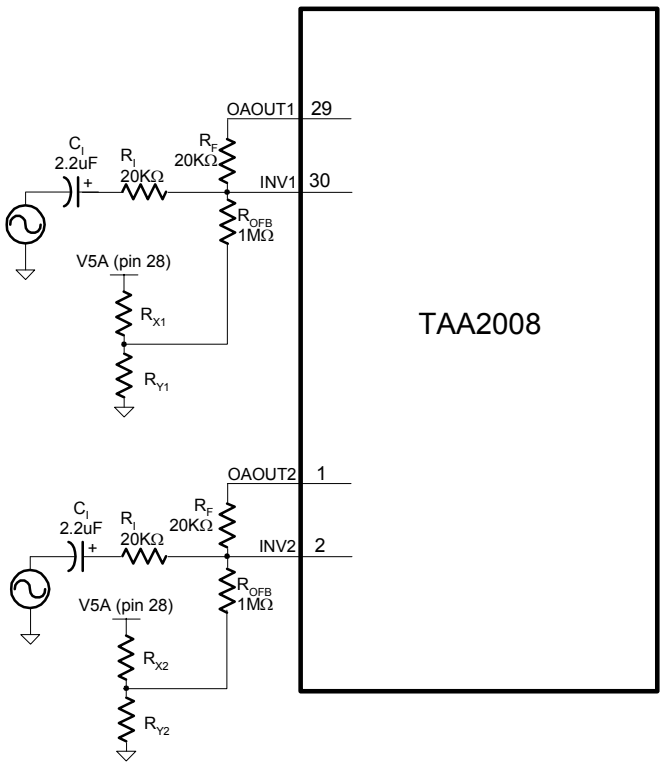
The DC offset voltages that appear at the speaker terminals of a TAA2008 amplifier are typically small and for most applications no DC offset correction is necessary. The TAA2008 is 100% tested to ensure that the differential output DC offset voltage is less than +/-150mV. However this DC offset can cause a small turn on and turn off pop, depending on the offset value for that specific IC. Every TAA2008 IC will have a different offset voltage for each channel.

If the output offset is deemed unacceptable from a turn on/off pop standpoint, there are three recommended methods for correcting it. These methods of trimming the offset voltage are optional and for most cases the additional circuitry is not needed.

1) A potentiometer can be used at the input of the TAA2008 as shown in the figure below. By changing the input bias voltage the output DC offset voltage can be trimmed. Two separate potentiometers must be used to trim both channels.



2) In cases where manually trimming potentiometers is not possible, resistors can be used in place of potentiometers. Since each TAA2008 has different offset voltage, the output offset voltage will need to be measured for both channel 1 and channel 2 and then resistors will have to be added on the PC board to trim the offset. Below is a lookup table for resistor values for corresponding offset voltages. Both Rx and Ry values should be 1% tolerance resistors. Please refer to the EB-TAA2008 document for more information on this manual trim method using resistors.



OFFSET	Ry	Rx (1%)
150mV	20kΩ	13.3kΩ
140mV	20kΩ	13.7kΩ
130mV	20kΩ	14.3kΩ
120mV	20kΩ	14.7kΩ
110mV	20kΩ	15.4kΩ
100mV	20kΩ	15.8kΩ
90mV	20kΩ	16.2kΩ
80mV	20kΩ	16.9kΩ
70mV	20kΩ	17.4kΩ
60mV	20kΩ	17.8kΩ
50mV	20kΩ	18.7kΩ
40mV	20kΩ	19.1kΩ
30mV	20kΩ	19.6kΩ
20mV	20kΩ	20.5kΩ
10mV	20kΩ	21kΩ
0mV	20kΩ	21.5kΩ
-10mV	20kΩ	22.6kΩ
-20mV	20kΩ	23.2kΩ
-30mV	20kΩ	24.3kΩ
-40mV	20kΩ	24.9kΩ
-50mV	20kΩ	25.5kΩ
-60mV	20kΩ	26.7kΩ
-70mV	20kΩ	27.4kΩ
-80mV	20kΩ	28.0kΩ
-90mV	20kΩ	29.4kΩ
-100mV	20kΩ	30.1kΩ
-110mV	20kΩ	31.6kΩ
-120mV	20kΩ	32.4kΩ
-130mV	20kΩ	33.2kΩ
-140mV	20kΩ	34.8kΩ
-150mV	20kΩ	35.7kΩ

3) A DC servo using a dual op amp can also be used to automatically null any offset voltage. This DC servo will only eliminate the turn off pop since the RC time constant of the DC servo is very slow. Please contact Tripath sales for additional information on the DC servo circuit.

Power Dissipation Derating

The TAA2008, as a result of high efficiency and good package thermal characteristics, can operate at elevated ambient temperatures without having to derate the output power, assuming 8 ohm output loads or higher. This in stark contrast to many other “competitive” solutions from other semiconductor vendors, many of which can only provide full power at ambient temperatures of 25°C, or slightly higher, without exceeding a junction temperature of 150°C. Lower die temperatures result in a more robust and reliable amplifier solution that can only be facilitated by a combination of high efficiency and good package thermal characteristics.

The exposed pad must be soldered to the PC Board to increase the maximum power dissipation capability of the TAA2008 package. Soldering will minimize the likelihood of an over-temperature fault occurring during continuous heavy load conditions. There should be vias for connecting the exposed pad to the copper area on the printed circuit board.

Conducting initial testing or characterization ***without*** the exposed pad soldered to the printed circuit board will give erroneous case temperature measurements. The TAA2008 is an extremely robust device, so not soldering the device to the printed circuit board, due to potential rework issues, should not be a concern. These devices do not fail unless the operating supply voltages maximums are exceeded, and/or an improper printed board design is utilized.

The maximum device power dissipation, for a given ambient temperature, can be calculated based on a 150°C maximum junction temperature, T_{JMAX}, as given by the following equation:

$$P_{DISS} = \frac{(T_{JMAX} - T_A)}{\theta_{JA}}$$

where:

P_{DISS} = maximum power dissipation
T_{JMAX} = maximum junction temperature of TAA2008
T_A = operating ambient temperature
θ_{JA} = junction-to-ambient thermal resistance = 22°C/W when soldered to PCB

From the above formula, the maximum power dissipation at an ambient temperature of 25°C is 5.68W, and at 70°C is 3.64W.

The amount of power dissipation can easily be calculated given the output power and efficiency for that output level. The Typical Performance Characteristics section has a significant amount of efficiency and power dissipation data. The relation between P_{DISS}, Output Power and Efficiency is given in the formula below.

$$P_{DISS} = \frac{\text{Total Output Power}}{\text{Efficiency}} - \text{Total Output Power}$$

The efficiency for the TAA2008 is 86% at 9 watts per channel. Thus, the power dissipation is:

$$P_{DISS} = \frac{18W}{0.86} - 18W = 2.93 \text{ Watts}$$

Since 2.93 Watts is less than the maximum power dissipation of 3.64 Watts at 70°C, the TAA2008 is not thermally limited assuming maximum output power into 8 ohms loads.

The resultant junction temperature, T_J, can be calculated using the formula below:

$$T_J = P_{DISS} * \Theta_{JA} + T_A$$

The power dissipation at 9 watts per channel into 8 ohms is 2.93W, as calculated above. Assuming an ambient temperature of 40°C, this results in a junction temperature of 105°C. This junction temperature is much lower than “competitive” solutions at similar output power levels with 8 ohm loads, resulting in a more reliable amplifier design.

A similar set of calculations can be done for a 16 ohm load. But since the efficiency is higher and the output power is lower for a 16 ohm load, as opposed to an 8 ohm load, the power dissipation will be smaller. Since the TAA2008 is not thermally limited into 8 ohm loads, it will not be thermal limited into 16 ohm loads.

Performance Measurements of the TAA2008

The TAA2008 operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an

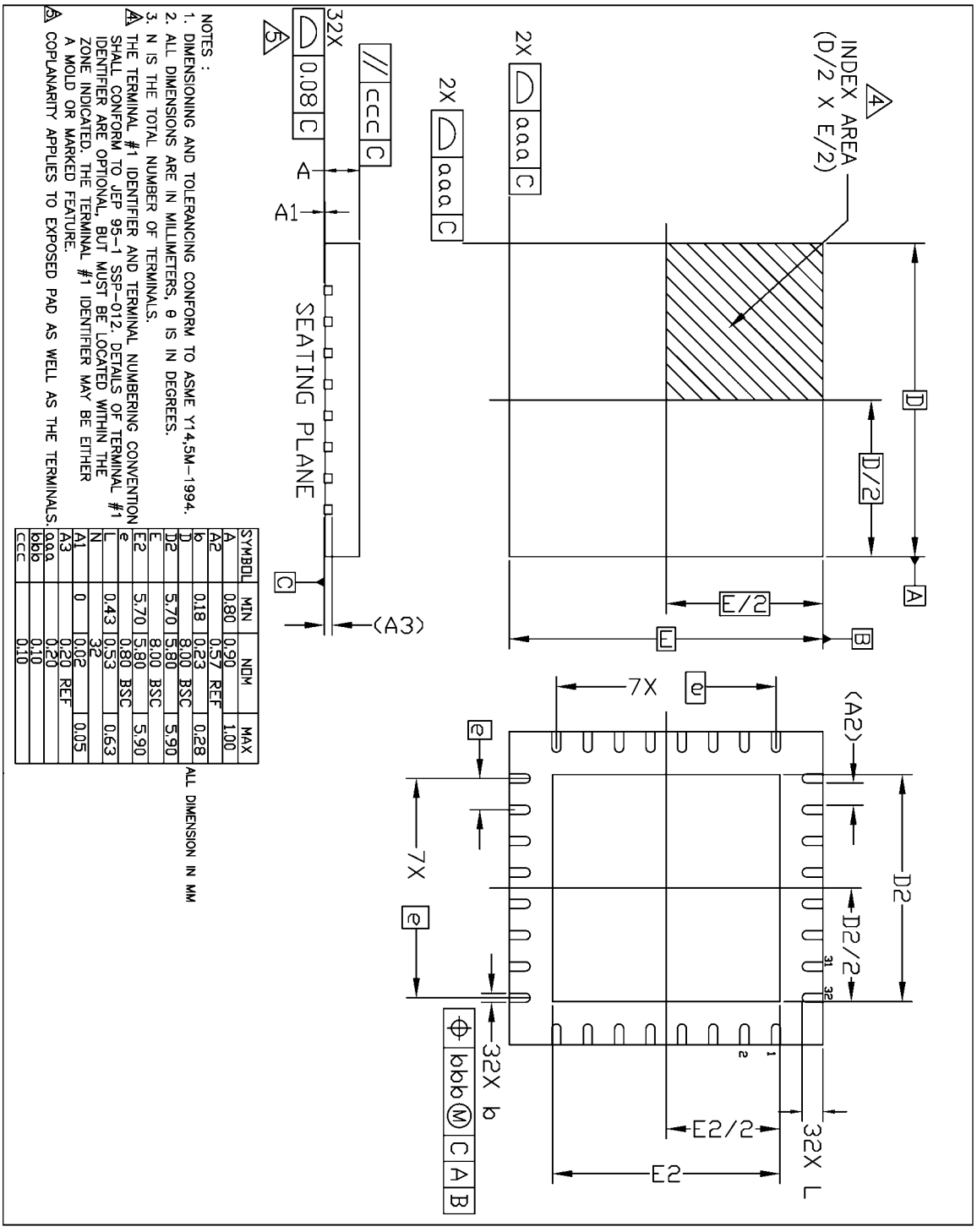
amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 100kHz and 1.0MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the Tripath amplifiers switching pattern will degrade the measurement.

One feature of the TAA2008 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TAA2008 Evaluation Board uses the Test/Application Circuit in this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

PACKAGE INFORMATION

32 PIN QFN - 8MM x 8MM X 1MM



NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP 95-1 SSP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

5. COPLANARITY APPLIES TO EXPOSED PAD AS WELL AS THE TERMINALS.

SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.28
D		8.00 BSC	
D2	5.70	5.80	5.90
E		8.00 BSC	
E2	5.70	5.80	5.90
e		0.80 BSC	
L	0.43	0.53	0.63
N		32	
A1	0	0.02	0.05
A3		0.20 REF	
aaa		0.20	
bbb		0.10	
ccc		0.10	

ALL DIMENSION IN MM

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Contact Information

TRIPATH TECHNOLOGY, INC

2560 Orchard Parkway, San Jose, CA 95131
408.750.3000 - P
408.750.3001 - F

For more Sales Information, please visit us @ www.tripath.com/cont_s.htm
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